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EXAMINER
MOVVA, AMAR

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/749,130	PAVAN ET AL.	
	Examiner	Art Unit	
	AMAR MOVVA	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,15-26 and 31-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,15-26 and 31-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 2 is objected to because of the following informalities: please amend as follows "Said floating gate regions are covered by a dielectric layer before being insulated from each other through said dielectric ~~layer~~ region with low dielectric constant value"

2. Claim 19 is objected to because of the following informalities: please amend as follows "~~A~~ The control gate region capacitively coupled to the floating gate region through a dielectric layer"

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim1-4,15-24, and 31-38 are rejected under 35 U.S.C. 102(e) as being anticipated by Tripsas '945.

a. Regarding claims 1-4.,15, and 35 , Tripsas discloses a non-volatile memory cell integrated on a semiconductor substrate (14, fig. 1) and comprising: a floating gate transistor including a source region and a drain region (34,35, fig.

2), a gate region projecting from the substrate and comprised between said source and drain regions, said gate region having a predetermined length and width and comprising a first floating gate region (20,72, fig. 1) and a control gate region (31, fig. 1), wherein said floating gate region is insulated laterally, along a direction orthogonal to a plane including the floating gate, source, and drain regions, by a dielectric region (56, fig. 1) with a low dielectric constant value that is formed under the control gate region and between adjacent floating gate regions (col. 4). Said floating gate regions are covered by a dielectric layer (28, fig. 1) before being insulated from each other through said dielectric region with low dielectric constant value (fig. 1, See Below). Said dielectric layer with low dielectric constant value is bounded between said floating gate regions (fig. 1). Said dielectric layer with low dielectric constant value is formed by a layer of material having a dielectric constant comprised between 1 and 3.9 (fig. 1). A memory cell matrix formed on a semiconductor substrate comprising a plurality of memory cells organized in rows and columns (fig. 1,2), each cell in a given row being coupled to a corresponding word line and each cell being formed according to claim 1 (fig. 1,2), the cell matrix being wherein adjacent memory cells being coupled to a same word line of said memory cell matrix are insulated from each other by a dielectric layer with low dielectric constant value. The dielectric layer completely fills a space between adjacent memory cells coupled to the same word line (fig. 1).

b. Regarding claims 16-20 and 36 , Tripsas discloses a memory-cell structure formed on a semiconductor substrate (1, fig. 1), the memory-cell structure comprising a plurality of non- volatile memory cells arranged in rows and columns and formed on the semiconductor substrate, (fig. 2) each memory cell in a respective row being coupled to a corresponding word line and each memory cell including a floating gate region (18, fig. 1) and a control gate region (31, fig. 1), the memory-cell structure including an insulating region (56, fig. 1) having a relatively low dielectric constant formed between adjacent floating gate regions of the memory cells in a row that are coupled to the same word line and under the control gate region. A dielectric layer (28, fig. 1) having a greater dielectric constant than the insulating regions formed on the floating gate regions. The insulating layer has a dielectric constant having a value of between approximately 1 and approximately 3.9 (col. 7). A control gate region capacitively coupled to the floating gate region through a dielectric layer having a dielectric constant greater than that of the insulating layer, and wherein the control gate regions of memory cells in respective rows are electrically interconnected (fig. 1). Each memory cell comprises a FLASH memory cell (fig. 1). The dielectric layer completely fills a space between adjacent memory cells coupled to the same word line (fig. 1).

c. Regarding claims 21-23 and 37 , Tripsas discloses a memory device, comprising: a memory-cell array formed on a semiconductor substrate (1, fig. 1), the memory- cell array comprising a plurality of non-volatile memory cells

arranged in rows and columns and formed on the semiconductor substrate (fig. 1,2), each memory cell in a respective row being coupled to a corresponding word line (fig. 2) and each memory cell including a floating gate region (18, fig. 1) and a control gate region (31, fig. 1), the memory-cell array including an insulating region (56, fig. 1) having a relatively low dielectric constant formed between adjacent floating gate regions of the memory cells in a row that are coupled to the same word line and under the control gate region (fig. 1). The memory device comprises a FLASH memory device and each memory cell comprises a FLASH memory cell (fig. 1). A dielectric layer (18, fig. 1) having a greater dielectric constant than the insulating regions formed on the floating gate regions. The dielectric layer completely fills a space between adjacent memory cells coupled to the same word line (fig. 1).

d. Regarding claims 24 and 38 , Tripsas discloses an electronic system, comprising: a memory device including, a memory-cell array formed on a semiconductor substrate (1, fig. 1), the memory-cell array comprising a plurality of non-volatile memory cells arranged in rows and columns and formed on the semiconductor substrate (fig. 1,2), each memory cell in a respective row being coupled to a corresponding word line and each memory cell and including a floating gate (18, fig. 1) region and a control gate region (31, fig. 1), the memory-cell array including an insulating region (56, fig. 1) having a relatively low dielectric constant formed between adjacent floating gate regions of the memory cells in a row that are coupled to the same word line and under the control gate

region. The electronic system comprises a computer system (col. 1). The memory device comprises a FLASH memory device and each memory cell comprises a FLASH memory cell (fig. 1). The dielectric layer completely fills a space between adjacent memory cells coupled to the same word line (fig. 1).

e. Regarding claims 31-34 , Tripsas discloses a memory-cell structure formed on a semiconductor substrate (1, fig. 1), the memory-cell structure comprising a plurality of non- volatile memory cells arranged in rows and columns and formed on the semiconductor substrate (fig. 1,2), each memory cell in a respective row being coupled to a corresponding word line and each memory cell including a gate structure having a floating gate region (18, fig.1) and a control gate region (31, fig. 1), the memory-cell structure including an insulating region (56, fig. 1) having a relatively low dielectric constant formed between adjacent floating gate regions of the memory cells in a row that are coupled to the same word line (fig. 1), the insulating region having a first side in direct contact with a first one of the adjacent floating gate regions and a second side in direct contact with a second one of the adjacent floating gate regions, and the insulating region being formed under the control gate region (fig. 1). A dielectric layer (28, fig. 1) having a greater dielectric constant than the insulating region formed between adjacent floating gate regions, the dielectric layer being formed on the insulating region and on the floating gate regions (fig. 1). The insulating region has a dielectric constant having a value of between approximately 1 and

approximately 3.9 (col. 7). Each memory cell comprises a FLASH memory cell (fig. 1).

Please Note: Claim(s) 2 contain(s) process limitations "Said floating gate regions are covered by a dielectric layer before being insulated from each other through said dielectric region with low dielectric constant value". These limitations invoke the Product-by-Process doctrine. Product-by-process limitations are not limited by the manipulations of the recited steps, only the structure implied by the steps (MPEP 2113). Specifically forming the dielectric layer first before being insulated by the dielectric region does not appear to structurally distinguish the invention over the resulting structure produced by the prior art. The burden to show that the claimed method necessarily distinguishes over the prior art is on the applicant.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tripas '945 in view of Liu'063.

a. Tripas discloses the device of claim 1 but does not expressly disclose that the dielectric region is a low-k silicon oxide layer doped with fluorine.

b. Liu discloses a non-volatile memory cell wherein floating gates are are separated laterally via a low-k silicon oxide doped with fluorine (48/42, fig. 8a-9b, lines 27-33, col. 6).

c. It would have been obvious to one of ordinary skill in the art at the time of the invention to have used Liu's low-k silicon oxide layer doped with fluorine in Tripsas' dielectric layer in order to reduce capacitive coupling between the respective floating gates (lines 27-33, col. 6 of Liu).

2. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tripas '945 in view of Ahn '132.

a. Tripas discloses the device of claim 1 but does not expressly disclose that the dielectric region is a low-k carbon oxide alkyl layer.

b. Ahn discloses a semiconductor device wherein the gate is insulated laterally from other gates via a low-k carbon oxide alkyl layer (140, fig. 3,[0019[0020])

c. It would have been obvious to one of ordinary skill in the art at the time of the invention to have used Ahn's low-k carbon oxide alkyl layer in Tripsas' dielectric layer in order to reduce capacitive coupling between the respective floating gates (lines 27-33, col. 6 of Liu).

2. Claims 25 and 26 rejected under 35 U.S.C. 103(a) as being unpatentable over Tripas '945.

a. Tripas discloses the device of claim 24 and that the memory device is a FLASH memory device with FLASH memory cells. Tripas, however, does not expressly disclose that the electronic system has a computer system.

b. It was conventional in the industry at the time of the invention to make electronic systems with memory devices placed in computer systems. Therefore it would have been obvious for the electronic system to have had a computer system in order to make use of the memory cell.

Response to Arguments

2. Applicant's arguments filed 5-30-08 have been fully considered but they are not fully persuasive.

a. Applicant argues that use of the Ahn reference in combination with the primary reference is inappropriate since it does not apply to FLASH memory. Examiner notes, however, that alleviating parasitic capacitance between conductors is a problem in numerous semiconductor devices (e.g. FETS) not solely FLASH memory. Therefore give the motivation described above one of ordinary skill in the art would look to a variety of semiconductor devices in order to reduce parasitic capacitance.

b. Applicant argues that a porous dielectric could not be applied to the FLASH memory due to poor contamination resistance. Even assuming *arguendo* that we assume attorney's arguments, which are not supported by factual evidence, have some factual basis, poor contamination resistance is not specific

to FLASH memory devices. Specifically said poor contamination resistance would likewise afflict the Ahn reference as well. Since it is clear that Ahn using said dielectric provides for workable device, one of ordinary skill would recognize use of said dielectric in Tripsas' device to reduce parasitic capacitance.

c. Applicant argues that orientation of Ahn's dielectric prevents a combination with the Tripsas' device. Examiner notes Tripsas' dielectric region is only being materially modified not structurally modified to reduce parasitic capcitance.

d. Applicant's remaining arguments have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AMAR MOVVA whose telephone number is (571)272-9009. The examiner can normally be reached on 7:30 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Amar Movva
Examiner
Art Unit 2891

Am

/Bradley K Smith/
Primary Examiner, Art Unit 2894